ELECTROSTATIC DISCHARGE (ESD) TESTING REPORT

Applicant/Department: RAIO TECHNOLOGY INC.	
Product: RA8877	**LOT:**
Case NO: B150608046	**Quantity:** 18 ea
Test Item: Human Body Model (HBM)	**Package/Pin Count:** LQFP-128(14*14)
Application Date: 2015/6/10	**Date Finished:** 2015/6/10
Reference: JEDEC JS-001-2010	**Temperature:** 25 ± 5 °C **Humidity:** 55 ± 5%
Test Instrument: JB_ZAP-B	**Test Voltage:** PD/ND/PS/NS (±)2000V , (±)4000V , (±)5000V VDD(+)-VSS / VDD(-)-VSS (±)1000V ~ (±)5000V Step: (±)1000V
Failure Criteria: After testing, DUT no longer fulfills requirements of ± 30% voltage drift at ± 1uA reference current and compliance within 10% V+I envelope around REFERENCE I-V curve (pre-zap).	
File Name of Raw Data: 50610A_E	
ESD Testing Result: Minimum Pass Level = ±2000V	

NOTE 1: ESD/latch-up test is employed as one of qualification tests for electronic products. However, the pass / fail results of this test can NOT be taken as go/no-go criteria for IC tape-out and mass production. Before and after ESD/latch-up test(s), complete parametric and functional testing (F/T) are essential for determining pass/fail of the tested products. (References: Page 9, AEC-Q100-003-Rev-E-2003; and Page 15, ESDA-JEDEC JS-001-2011).

NOTE 2: MA-tek sample storage policy is 14 days after the test data delivery. Prolonged storage can be arranged per client's request.

WE HEREBY CERTIFY THAT:

The test(s) was/were conducted according to test conditions provided by customer.Testing was performed on calibrated and JEDEC-ESDA qualified ESD instruments.The quality and comprehensiveness of this test(s) were delivered by qualified personnel.

Tested by	Reviewed by	Approved by
Marco Han	Andy Wang	Edward Hu

CERTIFICATE of APPROVAL INDEPENDENT TESTING LABORATORY:

ISO9001:2008 Certificate Registration No. 20001845 QM08, issued by UL DQS Inc.
IEC/IECQ17025 Certificate No. IECQ-L ULTW 09.0009, approved by Certification Body (CB): UL Registered Firm

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1. TEST SUMMARY

Sensitivity Pass: ±2000V

Class-2

JEDEC JS-001-2010

Class-0A : 0 V - < 125 V
Class-0B : 125 V - < 250 V
Class-1A : 250 V - < 499 V
Class-1B : 500 V - < 999 V
Class-1C : 1000 V - < 1999 V
Class-2 : 2000 V - < 3999 V
Class-3A : 4000 V - < 7999 V
Class-3B : >= 8000 V

Pin Combination	Sample	Pass Level
IO(+)-Power	3	+5000V
IO(-)-Power	3	-5000V
IO(+)-Ground	3	+5000V
IO(-)-Ground	3	-5000V
Power(+)-Ground	3	+2000V
Power(-)-Ground	3	-5000V

* DUT failed at the first level of test condition, defined by client.

NOTE: Red color in raw data indicates failed pins, if any.

2. Pin ASSIGNMENT

Pin Group	PAD Pins
IO	1 , 2 , 6 , 7 , 8 , 9 , 10 , 11 , 12 , 13 , 14 , 15 , 16 , 17 , 18 , 19 , 20 , 21 , 22 , 25 , 26 , 27 , 28 , 29 , 30 , 31 , 32 , 33 , 34 , 35 , 36 , 37 , 38 , 39 , 40 , 41 , 44 , 45 , 46 , 47 , 48 , 49 , 50 , 51 , 52 , 53 , 54 , 55 , 56 , 57 , 58 , 59 , 60 , 61 , 65 , 66 , 67 , 68 , 69 , 70 , 71 , 72 , 73 , 74 , 77 , 78 , 79 , 80 , 81 , 82 , 83 , 84 , 85 , 86 , 87 , 90 , 91 , 92 , 93 , 94 , 95 , 96 , 99 , 100 , 101 , 102 , 103 , 108 , 109 , 110 , 111 , 112 , 113 , 116 , 117 , 118 , 119 , 120 , 121 , 122 , 125 , 126 , 127 , 128
AVDD33	114
AVSSIO	115
LDO_CAP12	4 , 63 , 106
VDD33	3 , 23 , 42 , 62 , 75 , 88 , 97 , 104 , 123
VSS	5 , 24 , 43 , 64 , 76 , 89 , 98 , 105 , 107 , 124
	Ground=AVSSIO,VSS
	Power=AVDD33,LDO_CAP12,VDD33

3. ESD TEST CONDITIONS

ESD Zap Interval: **≧ 500 mS** **Zap:** **1 pulse.**

Testing Combinations

IO(+)-Power
IO(-)-Power
IO(+)-Ground
IO(-)-Ground
Power(+)-Ground
Power(-)-Ground

4. Raw Data - 2

IO(+)-Power(Unit: V)											
Test Pin Fail Voltage			#01	#02	#03	Test Pin Fail Voltage			#01	#02	#03
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
6	XTEST[2:0]	6	Pass	Pass	Pass	7	XTEST[2:0]	7	Pass	Pass	Pass
8	XTEST[2:0]	8	Pass	Pass	Pass	9	XPS[2:0]	9	Pass	Pass	Pass
10	XPS[2:0]	10	Pass	Pass	Pass	11	XPS[2:0]	11	Pass	Pass	Pass
12	XnRST	12	Pass	Pass	Pass	13	XnCS	13	Pass	Pass	Pass
14	XnRD_EN	14	Pass	Pass	Pass	15	XnWR_RWN	15	Pass	Pass	Pass
16	XA0	16	Pass	Pass	Pass	17	XnWAIT	17	Pass	Pass	Pass
18	XDB[0:4]	18	Pass	Pass	Pass	19	XDB[0:4]	19	Pass	Pass	Pass
20	XDB[0:4]	20	Pass	Pass	Pass	21	XDB[0:4]	21	Pass	Pass	Pass
22	XDB[0:4]	22	Pass	Pass	Pass	25	XDB[5:15]	25	Pass	Pass	Pass
26	XDB[5:15]	26	Pass	Pass	Pass	27	XDB[5:15]	27	Pass	Pass	Pass
28	XDB[5:15]	28	Pass	Pass	Pass	29	XDB[5:15]	29	Pass	Pass	Pass
30	XDB[5:15]	30	Pass	Pass	Pass	31	XDB[5:15]	31	Pass	Pass	Pass
32	XDB[5:15]	32	Pass	Pass	Pass	33	XDB[5:15]	33	Pass	Pass	Pass
34	XDB[5:15]	34	Pass	Pass	Pass	35	XDB[5:15]	35	Pass	Pass	Pass
36	XnINTR	36	Pass	Pass	Pass	37	XnSFCS[0:1]	37	Pass	Pass	Pass
38	XnSFCS[0:1]	38	Pass	Pass	Pass	39	XSCK	39	Pass	Pass	Pass
40	XMOSI	40	Pass	Pass	Pass	41	XMISO	41	Pass	Pass	Pass
44	XMBA[1:0]	44	Pass	Pass	Pass	45	XMBA[1:0]	45	Pass	Pass	Pass
46	XMA[12:0]	46	Pass	Pass	Pass	47	XMA[12:0]	47	Pass	Pass	Pass
48	XMA[12:0]	48	Pass	Pass	Pass	49	XMA[12:0]	49	Pass	Pass	Pass
50	XMA[12:0]	50	Pass	Pass	Pass	51	XMA[12:0]	51	Pass	Pass	Pass
52	XMA[12:0]	52	Pass	Pass	Pass	53	XMA[12:0]	53	Pass	Pass	Pass
54	XMA[12:0]	54	Pass	Pass	Pass	55	XMA[12:0]	55	Pass	Pass	Pass
56	XMA[12:0]	56	Pass	Pass	Pass	57	XMA[12:0]	57	Pass	Pass	Pass
58	XMA[12:0]	58	Pass	Pass	Pass	59	XNMCS	59	Pass	Pass	Pass
60	XMCKE	60	Pass	Pass	Pass	61	XMCLK	61	Pass	Pass	Pass
65	XnMCAS	65	Pass	Pass	Pass	66	XnMRAS	66	Pass	Pass	Pass
67	XnMWR	67	Pass	Pass	Pass	68	XMDQM0	68	Pass	Pass	Pass
69	XMD[0:5]	69	Pass	Pass	Pass	70	XMD[0:5]	70	Pass	Pass	Pass
71	XMD[0:5]	71	Pass	Pass	Pass	72	XMD[0:5]	72	Pass	Pass	Pass
73	XMD[0:5]	73	Pass	Pass	Pass	74	XMD[0:5]	74	Pass	Pass	Pass
77	XMD[6:7]	77	Pass	Pass	Pass	78	XMD[6:7]	78	Pass	Pass	Pass
79	XMDQM1	79	Pass	Pass	Pass	80	XMD[8:15]	80	Pass	Pass	Pass
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	Pass	Pass	Pass
83	XMD[8:15]	83	Pass	Pass	Pass	84	XMD[8:15]	84	Pass	Pass	Pass
85	XMD[8:15]	85	Pass	Pass	Pass	86	XMD[8:15]	86	Pass	Pass	Pass
87	XMD[8:15]	87	Pass	Pass	Pass	90	XPWM[0:1]	90	Pass	Pass	Pass
91	XPWM[0:1]	91	Pass	Pass	Pass	92	XKIN[0:4]	92	Pass	Pass	Pass
93	XKIN[0:4]	93	Pass	Pass	Pass	94	XKIN[0:4]	94	Pass	Pass	Pass
95	XKIN[0:4]	95	Pass	Pass	Pass	96	XKIN[0:4]	96	Pass	Pass	Pass
99	XGPIO_D[0:1]	99	Pass	Pass	Pass	100	XGPIO_D[0:1]	100	Pass	Pass	Pass
101	XGPIO_D6	101	Pass	Pass	Pass	102	XGPIO_D[2:3]	102	Pass	Pass	Pass
103	XGPIO_D[2:3]	103	Pass	Pass	Pass	108	XTX3N/P	108	Pass	Pass	Pass
109	XTX3N/P	109	Pass	Pass	Pass	110	XTX2N/P	110	Pass	Pass	Pass

4. Raw Data - 2

IO(+)-Power(Unit: V)											
Test Pin Fail Voltage			#01	#02	#03	Test Pin Fail Voltage			#01	#02	#03
111	XTX2N/P	111	Pass	Pass	Pass	112	XCKN/P	112	Pass	Pass	Pass
113	XCKN/P	113	Pass	Pass	Pass	116	XTX1N/P	116	Pass	Pass	Pass
117	XTX1N/P	117	Pass	Pass	Pass	118	XTX0N/P	118	Pass	Pass	Pass
119	XTX0N/P	119	Pass	Pass	Pass	120	XGPIO_D[4:5]	120	Pass	Pass	Pass
121	XGPIO_D[4:5]	121	Pass	Pass	Pass	122	XGPIO_D7	122	Pass	Pass	Pass
125	XKOUT[0:3]	125	Pass	Pass	Pass	126	XKOUT[0:3]	126	Pass	Pass	Pass
127	XKOUT[0:3]	127	Pass	Pass	Pass	128	XKOUT[0:3]	128	Pass	Pass	Pass

4. Raw Data - 2

IO(-)-Power(Unit: V)											
Test Pin Fail Voltage			#04	#05	#06	Test Pin Fail Voltage			#04	#05	#06
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
6	XTEST[2:0]	6	Pass	Pass	Pass	7	XTEST[2:0]	7	Pass	Pass	Pass
8	XTEST[2:0]	8	Pass	Pass	Pass	9	XPS[2:0]	9	Pass	Pass	Pass
10	XPS[2:0]	10	Pass	Pass	Pass	11	XPS[2:0]	11	Pass	Pass	Pass
12	XnRST	12	Pass	Pass	Pass	13	XnCS	13	Pass	Pass	Pass
14	XnRD_EN	14	Pass	Pass	Pass	15	XnWR_RWN	15	Pass	Pass	Pass
16	XA0	16	Pass	Pass	Pass	17	XnWAIT	17	Pass	Pass	Pass
18	XDB[0:4]	18	Pass	Pass	Pass	19	XDB[0:4]	19	Pass	Pass	Pass
20	XDB[0:4]	20	Pass	Pass	Pass	21	XDB[0:4]	21	Pass	Pass	Pass
22	XDB[0:4]	22	Pass	Pass	Pass	25	XDB[5:15]	25	Pass	Pass	Pass
26	XDB[5:15]	26	Pass	Pass	Pass	27	XDB[5:15]	27	Pass	Pass	Pass
28	XDB[5:15]	28	Pass	Pass	Pass	29	XDB[5:15]	29	Pass	Pass	Pass
30	XDB[5:15]	30	Pass	Pass	Pass	31	XDB[5:15]	31	Pass	Pass	Pass
32	XDB[5:15]	32	Pass	Pass	Pass	33	XDB[5:15]	33	Pass	Pass	Pass
34	XDB[5:15]	34	Pass	Pass	Pass	35	XDB[5:15]	35	Pass	Pass	Pass
36	XnINTR	36	Pass	Pass	Pass	37	XnSFCS[0:1]	37	Pass	Pass	Pass
38	XnSFCS[0:1]	38	Pass	Pass	Pass	39	XSCK	39	Pass	Pass	Pass
40	XMOSI	40	Pass	Pass	Pass	41	XMISO	41	Pass	Pass	Pass
44	XMBA[1:0]	44	Pass	Pass	Pass	45	XMBA[1:0]	45	Pass	Pass	Pass
46	XMA[12:0]	46	Pass	Pass	Pass	47	XMA[12:0]	47	Pass	Pass	Pass
48	XMA[12:0]	48	Pass	Pass	Pass	49	XMA[12:0]	49	Pass	Pass	Pass
50	XMA[12:0]	50	Pass	Pass	Pass	51	XMA[12:0]	51	Pass	Pass	Pass
52	XMA[12:0]	52	Pass	Pass	Pass	53	XMA[12:0]	53	Pass	Pass	Pass
54	XMA[12:0]	54	Pass	Pass	Pass	55	XMA[12:0]	55	Pass	Pass	Pass
56	XMA[12:0]	56	Pass	Pass	Pass	57	XMA[12:0]	57	Pass	Pass	Pass
58	XMA[12:0]	58	Pass	Pass	Pass	59	XNMCS	59	Pass	Pass	Pass
60	XMCKE	60	Pass	Pass	Pass	61	XMCLK	61	Pass	Pass	Pass
65	XnMCAS	65	Pass	Pass	Pass	66	XnMRAS	66	Pass	Pass	Pass
67	XnMWR	67	Pass	Pass	Pass	68	XMDQM0	68	Pass	Pass	Pass
69	XMD[0:5]	69	Pass	Pass	Pass	70	XMD[0:5]	70	Pass	Pass	Pass
71	XMD[0:5]	71	Pass	Pass	Pass	72	XMD[0:5]	72	Pass	Pass	Pass
73	XMD[0:5]	73	Pass	Pass	Pass	74	XMD[0:5]	74	Pass	Pass	Pass
77	XMD[6:7]	77	Pass	Pass	Pass	78	XMD[6:7]	78	Pass	Pass	Pass
79	XMDQM1	79	Pass	Pass	Pass	80	XMD[8:15]	80	Pass	Pass	Pass
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	Pass	Pass	Pass
83	XMD[8:15]	83	Pass	Pass	Pass	84	XMD[8:15]	84	Pass	Pass	Pass
85	XMD[8:15]	85	Pass	Pass	Pass	86	XMD[8:15]	86	Pass	Pass	Pass
87	XMD[8:15]	87	Pass	Pass	Pass	90	XPWM[0:1]	90	Pass	Pass	Pass
91	XPWM[0:1]	91	Pass	Pass	Pass	92	XKIN[0:4]	92	Pass	Pass	Pass
93	XKIN[0:4]	93	Pass	Pass	Pass	94	XKIN[0:4]	94	Pass	Pass	Pass
95	XKIN[0:4]	95	Pass	Pass	Pass	96	XKIN[0:4]	96	Pass	Pass	Pass
99	XGPIO_D[0:1]	99	Pass	Pass	Pass	100	XGPIO_D[0:1]	100	Pass	Pass	Pass
101	XGPIO_D6	101	Pass	Pass	Pass	102	XGPIO_D[2:3]	102	Pass	Pass	Pass
103	XGPIO_D[2:3]	103	Pass	Pass	Pass	108	XTX3N/P	108	Pass	Pass	Pass
109	XTX3N/P	109	Pass	Pass	Pass	110	XTX2N/P	110	Pass	Pass	Pass

4. Raw Data - 2

IO(-)-Power(Unit: V)											
Test Pin Fail Voltage			#04	#05	#06	Test Pin Fail Voltage			#04	#05	#06
111	XTX2N/P	111	Pass	Pass	Pass	112	XCKN/P	112	Pass	Pass	Pass
113	XCKN/P	113	Pass	Pass	Pass	116	XTX1N/P	116	Pass	Pass	Pass
117	XTX1N/P	117	Pass	Pass	Pass	118	XTX0N/P	118	Pass	Pass	Pass
119	XTX0N/P	119	Pass	Pass	Pass	120	XGPIO_D[4:5]	120	Pass	Pass	Pass
121	XGPIO_D[4:5]	121	Pass	Pass	Pass	122	XGPIO_D7	122	Pass	Pass	Pass
125	XKOUT[0:3]	125	Pass	Pass	Pass	126	XKOUT[0:3]	126	Pass	Pass	Pass
127	XKOUT[0:3]	127	Pass	Pass	Pass	128	XKOUT[0:3]	128	Pass	Pass	Pass

4. Raw Data - 2

IO(+)-Ground(Unit: V)											
Test Pin Fail Voltage			#07	#08	#09	Test Pin Fail Voltage			#07	#08	#09
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
6	XTEST[2:0]	6	Pass	Pass	Pass	7	XTEST[2:0]	7	Pass	Pass	Pass
8	XTEST[2:0]	8	Pass	Pass	Pass	9	XPS[2:0]	9	Pass	Pass	Pass
10	XPS[2:0]	10	Pass	Pass	Pass	11	XPS[2:0]	11	Pass	Pass	Pass
12	XnRST	12	Pass	Pass	Pass	13	XnCS	13	Pass	Pass	Pass
14	XnRD_EN	14	Pass	Pass	Pass	15	XnWR_RWN	15	Pass	Pass	Pass
16	XA0	16	Pass	Pass	Pass	17	XnWAIT	17	Pass	Pass	Pass
18	XDB[0:4]	18	Pass	Pass	Pass	19	XDB[0:4]	19	Pass	Pass	Pass
20	XDB[0:4]	20	Pass	Pass	Pass	21	XDB[0:4]	21	Pass	Pass	Pass
22	XDB[0:4]	22	Pass	Pass	Pass	25	XDB[5:15]	25	Pass	Pass	Pass
26	XDB[5:15]	26	Pass	Pass	Pass	27	XDB[5:15]	27	Pass	Pass	Pass
28	XDB[5:15]	28	Pass	Pass	Pass	29	XDB[5:15]	29	Pass	Pass	Pass
30	XDB[5:15]	30	Pass	Pass	Pass	31	XDB[5:15]	31	Pass	Pass	Pass
32	XDB[5:15]	32	Pass	Pass	Pass	33	XDB[5:15]	33	Pass	Pass	Pass
34	XDB[5:15]	34	Pass	Pass	Pass	35	XDB[5:15]	35	Pass	Pass	Pass
36	XnINTR	36	Pass	Pass	Pass	37	XnSFCS[0:1]	37	Pass	Pass	Pass
38	XnSFCS[0:1]	38	Pass	Pass	Pass	39	XSCK	39	Pass	Pass	Pass
40	XMOSI	40	Pass	Pass	Pass	41	XMISO	41	Pass	Pass	Pass
44	XMBA[1:0]	44	Pass	Pass	Pass	45	XMBA[1:0]	45	Pass	Pass	Pass
46	XMA[12:0]	46	Pass	Pass	Pass	47	XMA[12:0]	47	Pass	Pass	Pass
48	XMA[12:0]	48	Pass	Pass	Pass	49	XMA[12:0]	49	Pass	Pass	Pass
50	XMA[12:0]	50	Pass	Pass	Pass	51	XMA[12:0]	51	Pass	Pass	Pass
52	XMA[12:0]	52	Pass	Pass	Pass	53	XMA[12:0]	53	Pass	Pass	Pass
54	XMA[12:0]	54	Pass	Pass	Pass	55	XMA[12:0]	55	Pass	Pass	Pass
56	XMA[12:0]	56	Pass	Pass	Pass	57	XMA[12:0]	57	Pass	Pass	Pass
58	XMA[12:0]	58	Pass	Pass	Pass	59	XNMCS	59	Pass	Pass	Pass
60	XMCKE	60	Pass	Pass	Pass	61	XMCLK	61	Pass	Pass	Pass
65	XnMCAS	65	Pass	Pass	Pass	66	XnMRAS	66	Pass	Pass	Pass
67	XnMWR	67	Pass	Pass	Pass	68	XMDQM0	68	Pass	Pass	Pass
69	XMD[0:5]	69	Pass	Pass	Pass	70	XMD[0:5]	70	Pass	Pass	Pass
71	XMD[0:5]	71	Pass	Pass	Pass	72	XMD[0:5]	72	Pass	Pass	Pass
73	XMD[0:5]	73	Pass	Pass	Pass	74	XMD[0:5]	74	Pass	Pass	Pass
77	XMD[6:7]	77	Pass	Pass	Pass	78	XMD[6:7]	78	Pass	Pass	Pass
79	XMDQM1	79	Pass	Pass	Pass	80	XMD[8:15]	80	Pass	Pass	Pass
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	Pass	Pass	Pass
83	XMD[8:15]	83	Pass	Pass	Pass	84	XMD[8:15]	84	Pass	Pass	Pass
85	XMD[8:15]	85	Pass	Pass	Pass	86	XMD[8:15]	86	Pass	Pass	Pass
87	XMD[8:15]	87	Pass	Pass	Pass	90	XPWM[0:1]	90	Pass	Pass	Pass
91	XPWM[0:1]	91	Pass	Pass	Pass	92	XKIN[0:4]	92	Pass	Pass	Pass
93	XKIN[0:4]	93	Pass	Pass	Pass	94	XKIN[0:4]	94	Pass	Pass	Pass
95	XKIN[0:4]	95	Pass	Pass	Pass	96	XKIN[0:4]	96	Pass	Pass	Pass
99	XGPIO_D[0:1]	99	Pass	Pass	Pass	100	XGPIO_D[0:1]	100	Pass	Pass	Pass
101	XGPIO_D6	101	Pass	Pass	Pass	102	XGPIO_D[2:3]	102	Pass	Pass	Pass
103	XGPIO_D[2:3]	103	Pass	Pass	Pass	108	XTX3N/P	108	Pass	Pass	Pass
109	XTX3N/P	109	Pass	Pass	Pass	110	XTX2N/P	110	Pass	Pass	Pass

4. Raw Data - 2

IO(+)-Ground(Unit: V)											
Test Pin Fail Voltage			#07	#08	#09	Test Pin Fail Voltage			#07	#08	#09
111	XTX2N/P	111	Pass	Pass	Pass	112	XCKN/P	112	Pass	Pass	Pass
113	XCKN/P	113	Pass	Pass	Pass	116	XTX1N/P	116	Pass	Pass	Pass
117	XTX1N/P	117	Pass	Pass	Pass	118	XTX0N/P	118	Pass	Pass	Pass
119	XTX0N/P	119	Pass	Pass	Pass	120	XGPIO_D[4:5]	120	Pass	Pass	Pass
121	XGPIO_D[4:5]	121	Pass	Pass	Pass	122	XGPIO_D7	122	Pass	Pass	Pass
125	XKOUT[0:3]	125	Pass	Pass	Pass	126	XKOUT[0:3]	126	Pass	Pass	Pass
127	XKOUT[0:3]	127	Pass	Pass	Pass	128	XKOUT[0:3]	128	Pass	Pass	Pass

4. Raw Data - 2

IO(-)-Ground(Unit: V)											
Test Pin Fail Voltage			#10	#11	#12	Test Pin Fail Voltage			#10	#11	#12
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
6	XTEST[2:0]	6	Pass	Pass	Pass	7	XTEST[2:0]	7	Pass	Pass	Pass
8	XTEST[2:0]	8	Pass	Pass	Pass	9	XPS[2:0]	9	Pass	Pass	Pass
10	XPS[2:0]	10	Pass	Pass	Pass	11	XPS[2:0]	11	Pass	Pass	Pass
12	XnRST	12	Pass	Pass	Pass	13	XnCS	13	Pass	Pass	Pass
14	XnRD_EN	14	Pass	Pass	Pass	15	XnWR_RWN	15	Pass	Pass	Pass
16	XA0	16	Pass	Pass	Pass	17	XnWAIT	17	Pass	Pass	Pass
18	XDB[0:4]	18	Pass	Pass	Pass	19	XDB[0:4]	19	Pass	Pass	Pass
20	XDB[0:4]	20	Pass	Pass	Pass	21	XDB[0:4]	21	Pass	Pass	Pass
22	XDB[0:4]	22	Pass	Pass	Pass	25	XDB[5:15]	25	Pass	Pass	Pass
26	XDB[5:15]	26	Pass	Pass	Pass	27	XDB[5:15]	27	Pass	Pass	Pass
28	XDB[5:15]	28	Pass	Pass	Pass	29	XDB[5:15]	29	Pass	Pass	Pass
30	XDB[5:15]	30	Pass	Pass	Pass	31	XDB[5:15]	31	Pass	Pass	Pass
32	XDB[5:15]	32	Pass	Pass	Pass	33	XDB[5:15]	33	Pass	Pass	Pass
34	XDB[5:15]	34	Pass	Pass	Pass	35	XDB[5:15]	35	Pass	Pass	Pass
36	XnINTR	36	Pass	Pass	Pass	37	XnSFCS[0:1]	37	Pass	Pass	Pass
38	XnSFCS[0:1]	38	Pass	Pass	Pass	39	XSCK	39	Pass	Pass	Pass
40	XMOSI	40	Pass	Pass	Pass	41	XMISO	41	Pass	Pass	Pass
44	XMBA[1:0]	44	Pass	Pass	Pass	45	XMBA[1:0]	45	Pass	Pass	Pass
46	XMA[12:0]	46	Pass	Pass	Pass	47	XMA[12:0]	47	Pass	Pass	Pass
48	XMA[12:0]	48	Pass	Pass	Pass	49	XMA[12:0]	49	Pass	Pass	Pass
50	XMA[12:0]	50	Pass	Pass	Pass	51	XMA[12:0]	51	Pass	Pass	Pass
52	XMA[12:0]	52	Pass	Pass	Pass	53	XMA[12:0]	53	Pass	Pass	Pass
54	XMA[12:0]	54	Pass	Pass	Pass	55	XMA[12:0]	55	Pass	Pass	Pass
56	XMA[12:0]	56	Pass	Pass	Pass	57	XMA[12:0]	57	Pass	Pass	Pass
58	XMA[12:0]	58	Pass	Pass	Pass	59	XNMCS	59	Pass	Pass	Pass
60	XMCKE	60	Pass	Pass	Pass	61	XMCLK	61	Pass	Pass	Pass
65	XnMCAS	65	Pass	Pass	Pass	66	XnMRAS	66	Pass	Pass	Pass
67	XnMWR	67	Pass	Pass	Pass	68	XMDQM0	68	Pass	Pass	Pass
69	XMD[0:5]	69	Pass	Pass	Pass	70	XMD[0:5]	70	Pass	Pass	Pass
71	XMD[0:5]	71	Pass	Pass	Pass	72	XMD[0:5]	72	Pass	Pass	Pass
73	XMD[0:5]	73	Pass	Pass	Pass	74	XMD[0:5]	74	Pass	Pass	Pass
77	XMD[6:7]	77	Pass	Pass	Pass	78	XMD[6:7]	78	Pass	Pass	Pass
79	XMDQM1	79	Pass	Pass	Pass	80	XMD[8:15]	80	Pass	Pass	Pass
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	Pass	Pass	Pass
83	XMD[8:15]	83	Pass	Pass	Pass	84	XMD[8:15]	84	Pass	Pass	Pass
85	XMD[8:15]	85	Pass	Pass	Pass	86	XMD[8:15]	86	Pass	Pass	Pass
87	XMD[8:15]	87	Pass	Pass	Pass	90	XPWM[0:1]	90	Pass	Pass	Pass
91	XPWM[0:1]	91	Pass	Pass	Pass	92	XKIN[0:4]	92	Pass	Pass	Pass
93	XKIN[0:4]	93	Pass	Pass	Pass	94	XKIN[0:4]	94	Pass	Pass	Pass
95	XKIN[0:4]	95	Pass	Pass	Pass	96	XKIN[0:4]	96	Pass	Pass	Pass
99	XGPIO_D[0:1]	99	Pass	Pass	Pass	100	XGPIO_D[0:1]	100	Pass	Pass	Pass
101	XGPIO_D6	101	Pass	Pass	Pass	102	XGPIO_D[2:3]	102	Pass	Pass	Pass
103	XGPIO_D[2:3]	103	Pass	Pass	Pass	108	XTX3N/P	108	Pass	Pass	Pass
109	XTX3N/P	109	Pass	Pass	Pass	110	XTX2N/P	110	Pass	Pass	Pass

4. Raw Data - 2

IO(-)-Ground(Unit: V)											
Test Pin Fail Voltage			#10	#11	#12	Test Pin Fail Voltage			#10	#11	#12
111	XTX2N/P	111	Pass	Pass	Pass	112	XCKN/P	112	Pass	Pass	Pass
113	XCKN/P	113	Pass	Pass	Pass	116	XTX1N/P	116	Pass	Pass	Pass
117	XTX1N/P	117	Pass	Pass	Pass	118	XTX0N/P	118	Pass	Pass	Pass
119	XTX0N/P	119	Pass	Pass	Pass	120	XGPIO_D[4:5]	120	Pass	Pass	Pass
121	XGPIO_D[4:5]	121	Pass	Pass	Pass	122	XGPIO_D7	122	Pass	Pass	Pass
125	XKOUT[0:3]	125	Pass	Pass	Pass	126	XKOUT[0:3]	126	Pass	Pass	Pass
127	XKOUT[0:3]	127	Pass	Pass	Pass	128	XKOUT[0:3]	128	Pass	Pass	Pass

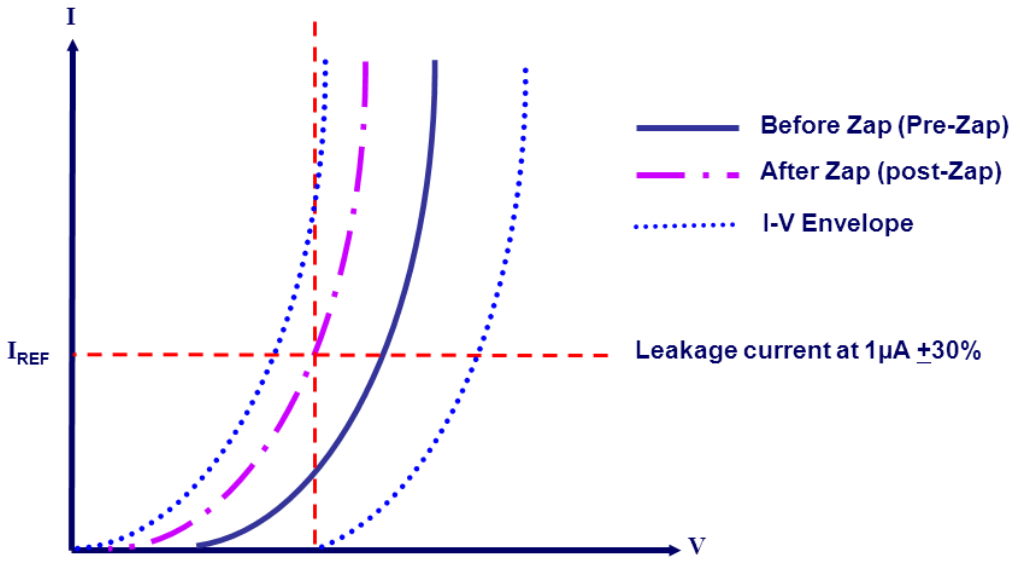
4. Raw Data - 2

Power(+)-Ground(Unit: V)											
Test Pin Fail Voltage			#13	#14	#15	Test Pin Fail Voltage			#13	#14	#15
3	VDD33	3	Pass	Pass	Pass	4	LDO_CAP12	4	Pass	Pass	Pass
23	VDD33	23	Pass	Pass	Pass	42	VDD33	42	Pass	Pass	Pass
62	VDD33	62	Pass	Pass	Pass	63	LDO_CAP12	63	Pass	Pass	Pass
75	VDD33	75	Pass	Pass	Pass	88	VDD33	88	Pass	Pass	Pass
97	VDD33	97	Pass	Pass	Pass	104	VDD33	104	Pass	Pass	Pass
106	LDO_CAP12	106	+3000	+5000	+4000	114	AVDD33	114	Pass	Pass	Pass
123	VDD33	123	Pass	Pass	Pass						

Power(-)-Ground(Unit: V)											
Test Pin Fail Voltage			#16	#17	#18	Test Pin Fail Voltage			#16	#17	#18
3	VDD33	3	Pass	Pass	Pass	4	LDO_CAP12	4	Pass	Pass	Pass
23	VDD33	23	Pass	Pass	Pass	42	VDD33	42	Pass	Pass	Pass
62	VDD33	62	Pass	Pass	Pass	63	LDO_CAP12	63	Pass	Pass	Pass
75	VDD33	75	Pass	Pass	Pass	88	VDD33	88	Pass	Pass	Pass
97	VDD33	97	Pass	Pass	Pass	104	VDD33	104	Pass	Pass	Pass
106	LDO_CAP12	106	Pass	Pass	Pass	114	AVDD33	114	Pass	Pass	Pass
123	VDD33	123	Pass	Pass	Pass						

5. APPENDIX-1 (PASS/FAIL CRITERIA)

FAILURE CRITERIA	**After testing, DUT no longer fulfills requirements of ± 30% voltage drift at ± 1uA reference current and compliance within 10% V+I envelope around REFERENCE I-V curve (pre-zap).**
Note	**For custom designed ESD testing customers may select variation in Idd, and leakage current as criteria to determine pass/fail results of ESD testing.**



Pass/Fail Criteria:
Variation of Leakage Current and I-V Shift in Pre-Zap and Post-Zap curves

6. APPENDIX-2 (ESD INSTRUMENTATION AT MA-TEK)

No.	Test Tools	Vendors	System Specification
1	Zapmaster	Thermo Keytek	256 Pin Count, ESD Pulse 50 V to 8 KV
2	MK2	Thermo Keytek	768 Pin Count, ESD Pulse 10 V to 8 KV
3	MK1	Thermo Scientific	256 Pin Count, ESD Pulse 10 V to 8 KV
4	CDM Tester	Oryx Orion	100 V to 2 KV
5	ESD Gun	Noiseken	Voltage = 1 V to 1 KV, Current = 10 nA to 20 A
6	High Temp. Test Module	Thermonics	Maximum temperature = 150°C.
7	TLP Tester	Thermo Scientific	Voltage = 1 V to 1 KV, Current = 10 nA to 20 A

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