Latch-up TESTING REPORT

Applicant/Department: RAIO TECHNOLOGY INC.	
Product: RA8877L4N	**LOT:**
Case NO: B150428022	**Quantity:** 12 ea
Test Item: Latch-up (LU)	**Package/Pin Count:** LQFP_128(14*14)
Application Date: 2015/04/28	**Date Finished:** 2015/05/15
Reference: JESD78D	**Temperature:** 85 ± 5 °C **Humidity:** 55 ± 5%
Test Instrument: JB_MK2-5	**Test Voltage:** 3.3V ~ 4.95V Step: 0.5V
Trigger Current: ±50mA ~ ±200mA Step: ±50mA ; ±125mA ~ ±125mA Step: ±0mA (2015.05.15加測)	
Failure Criteria: Device no longer meets the parts drawing requirements using parametric (1.4X INOM or INOM +10mA whichever is greater), functional or IV requirements.	
File Name of Raw Data: 50429B_L(RA8877L4N)	

NOTE 1: ESD/latch-up test is employed as one of qualification tests for electronic products. However, the pass / fail results of this test can NOT be taken as go/no-go criteria for IC tape-out and mass production. Before and after ESD/latch-up test(s), complete parametric and functional testing (F/T) are essential for determining pass/fail of the tested products. (References: Page 9, AEC-Q100-003-Rev-E-2003; and Page 15, ESDA-JEDEC JS-001-2011).

NOTE 2: MA-tek sample storage policy is 14 days after the test data delivery. Prolonged storage can be arranged per client's request.

WE HEREBY CERTIFY THAT:

The test(s) was/were conducted according to test conditions provided by customer.Testing was performed on calibrated and JEDEC-ESDA qualified ESD instruments.The quality and comprehensiveness of this test(s) were delivered by qualified personnel.

Tested by	Reviewed by	Approved by
yu kang	Jia Ming Lin	Edward Hu

CERTIFICATE of APPROVAL INDEPENDENT TESTING LABORATORY:

ISO9001:2008 Certificate Registration No. 20001845 QM08, issued by UL DQS Inc.
IEC/IECQ17025 Certificate No. IECQ-L ULTW 09.0009, approved by Certification Body (CB): UL Registered Firm

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1. TEST SUMMARY

IT CLASS: II

NOTE:

Class I - Latch-up testing performed at room temperature.

Class II - Latch-up testing performed at maximum ambient rated temperature for the device.

Trigger Model	Test Pin	Sample	Passing Current or Voltage
+IT	IP,IO,OP_3.3V	3	Pass(+100mA)
-IT	IP,IO,OP_3.3V	3	Pass(-200mA)
Vsupply Over voltage test	VDD3.3_3.3V	3	Pass(4.95V)
	AVDD33_3.3V		Pass(4.95V)
+IT	IP,IO,OP_3.3V Test For +125mA	3	Pass(+125mA)

* DUT failed at the first level of test condition, defined by client.

NOTE: Red color in raw data indicates failed pins, if any.

2. Pin ASSIGNMENT

Pin Group	PAD Pins
IO_3.3V	18 , 19 , 20 , 21 , 22 , 25 , 26 , 27 , 28 , 29 , 30 , 31 , 32 , 33 , 34 , 35 , 37 , 38 , 39 , 40 , 41 , 69 , 70 , 71 , 72 , 73 , 74 , 77 , 78 , 80 , 81 , 82 , 83 , 84 , 85 , 86 , 87 , 90 , 91 , 99 , 100 , 101 , 102 , 103 , 120 , 121 , 122
IP_3.3V	1 , 6 , 7 , 8 , 9 , 10 , 11 , 12 , 13 , 14 , 15 , 16 , 92 , 93 , 94 , 95 , 96
OP_3.3V	2 , 17 , 36 , 44 , 45 , 46 , 47 , 48 , 49 , 50 , 51 , 52 , 53 , 54 , 55 , 56 , 57 , 58 , 59 , 60 , 61 , 65 , 66 , 67 , 68 , 79 , 106 , 108 , 109 , 110 , 111 , 112 , 113 , 116 , 117 , 118 , 119 , 125 , 126 , 127 , 128
VDD33_3.3V	3 , 23 , 42 , 62 , 75 , 88 , 97 , 104 , 123
AVDD33_3.3V	114
VSS	5 , 24 , 43 , 64 , 76 , 89 , 98 , 105 , 107 , 124
AVSSIO	115

3. ESD TEST CONDITIONS

Testing Combinations

+IT
-IT
OV

4. Raw Data - 2

Positive Current Trigger(Unit:mA)											
Test Pin Fail Current			#01	#02	#03	Test Pin Fail Current			#01	#02	#03
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
4	LDO_CAP12	4	Pass	Pass	Pass	6	XTEST[2:0]	6	Pass	Pass	Pass
7	XTEST[2:0]	7	+150mA	+150mA	+150mA	8	XTEST[2:0]	8	+150mA	+150mA	+150mA
9	XPS[2:0]	9	+150mA	+150mA	+150mA	10	XPS[2:0]	10	+150mA	+150mA	+150mA
11	XPS[2:0]	11	+150mA	+150mA	+150mA	12	XnRST	12	+150mA	+150mA	+150mA
13	XnCS	13	+150mA	+150mA	+150mA	14	XnRD_EN	14	+150mA	+150mA	+150mA
15	XnWR_RWN	15	+150mA	+150mA	+150mA	16	XA0	16	+150mA	+150mA	+150mA
17	XnWAIT	17	+200mA	+200mA	+200mA	18	XDB[0:4]	18	+150mA	+150mA	+150mA
19	XDB[0:4]	19	+150mA	+150mA	+150mA	20	XDB[0:4]	20	+150mA	+150mA	+150mA
21	XDB[0:4]	21	+150mA	+150mA	+150mA	22	XDB[0:4]	22	+150mA	+150mA	+150mA
25	XDB[5:15]	25	+200mA	+200mA	+200mA	26	XDB[5:15]	26	+150mA	+150mA	+150mA
27	XDB[5:15]	27	+150mA	+150mA	+150mA	28	XDB[5:15]	28	+150mA	+150mA	+150mA
29	XDB[5:15]	29	+150mA	+150mA	+150mA	30	XDB[5:15]	30	+150mA	+150mA	+150mA
31	XDB[5:15]	31	+150mA	+150mA	+150mA	32	XDB[5:15]	32	+150mA	+150mA	+150mA
33	XDB[5:15]	33	+150mA	+150mA	+150mA	34	XDB[5:15]	34	+150mA	+150mA	+150mA
35	XDB[5:15]	35	+150mA	+150mA	+150mA	36	XnINTR	36	+200mA	+200mA	+200mA
37	XnSFCS[0:1]	37	+200mA	+200mA	+200mA	38	XnSFCS[0:1]	38	+200mA	+200mA	+200mA
39	XSCK	39	+150mA	+150mA	+150mA	40	XMOSI	40	+200mA	+200mA	+200mA
41	XMISO	41	+200mA	+200mA	+200mA	44	XMBA[1:0]	44	+200mA	+200mA	+200mA
45	XMBA[1:0]	45	+200mA	+200mA	+200mA	46	XMA[12:0]	46	+200mA	+200mA	+200mA
47	XMA[12:0]	47	+200mA	+200mA	+200mA	48	XMA[12:0]	48	+200mA	+200mA	+200mA
49	XMA[12:0]	49	+200mA	+200mA	+200mA	50	XMA[12:0]	50	+200mA	+200mA	+200mA
51	XMA[12:0]	51	+200mA	+200mA	+200mA	52	XMA[12:0]	52	+200mA	+200mA	+200mA
53	XMA[12:0]	53	+200mA	+200mA	+200mA	54	XMA[12:0]	54	+200mA	+200mA	+200mA
55	XMA[12:0]	55	+200mA	+200mA	+200mA	56	XMA[12:0]	56	+200mA	+200mA	+200mA
57	XMA[12:0]	57	+200mA	+200mA	+200mA	58	XMA[12:0]	58	+200mA	+200mA	+200mA
59	XNMCS	59	+200mA	+200mA	+200mA	60	XMCKE	60	+150mA	+150mA	+150mA
61	XMCLK	61	+200mA	+200mA	+200mA	63	LDO_CAP12	63	Pass	Pass	Pass
65	XnMCAS	65	+200mA	+200mA	+200mA	66	XnMRAS	66	+200mA	+200mA	+200mA
67	XnMWR	67	+200mA	+200mA	+200mA	68	XMDQM0	68	+200mA	+200mA	+200mA
69	XMD[0:5]	69	+150mA	+150mA	+150mA	70	XMD[0:5]	70	+150mA	+150mA	+150mA
71	XMD[0:5]	71	+150mA	+150mA	+150mA	72	XMD[0:5]	72	+150mA	+150mA	+150mA
73	XMD[0:5]	73	+150mA	+150mA	+150mA	74	XMD[0:5]	74	+150mA	+150mA	+150mA
77	XMD[6:7]	77	+200mA	+200mA	+200mA	78	XMD[6:7]	78	+200mA	+200mA	+200mA
79	XMDQM1	79	+200mA	+200mA	+200mA	80	XMD[8:15]	80	+150mA	+150mA	+150mA
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	+150mA	+150mA	+150mA
83	XMD[8:15]	83	+150mA	+150mA	+150mA	84	XMD[8:15]	84	+150mA	+150mA	+150mA
85	XMD[8:15]	85	+150mA	+150mA	+150mA	86	XMD[8:15]	86	+150mA	+150mA	+150mA
87	XMD[8:15]	87	+150mA	+150mA	+150mA	90	XPWM[0:1]	90	+200mA	+200mA	+200mA
91	XPWM[0:1]	91	+200mA	+200mA	+200mA	92	XKIN[0:4]	92	+150mA	+150mA	+150mA
93	XKIN[0:4]	93	+150mA	+150mA	+150mA	94	XKIN[0:4]	94	+150mA	+150mA	+150mA
95	XKIN[0:4]	95	+150mA	+150mA	+150mA	96	XKIN[0:4]	96	+150mA	+150mA	+150mA
99	XGPIO_D[0:1]	99	+200mA	+200mA	+200mA	100	XGPIO_D[0:1]	100	+150mA	+150mA	+150mA
101	XGPIO_D6	101	+150mA	+150mA	+150mA	102	XGPIO_D[2:3]	102	+150mA	+150mA	+150mA
103	XGPIO_D[2:3]	103	+150mA	+150mA	+150mA	106	LDO_CAP12	106	Pass	Pass	Pass

4. Raw Data - 2

Positive Current Trigger(Unit:mA)											
Test Pin Fail Current			#01	#02	#03	Test Pin Fail Current			#01	#02	#03
108	XTX3N/P	108	Pass	Pass	Pass	109	XTX3N/P	109	Pass	Pass	Pass
110	XTX2N/P	110	Pass	Pass	Pass	111	XTX2N/P	111	Pass	Pass	Pass
112	XCKN/P	112	Pass	Pass	Pass	113	XCKN/P	113	Pass	Pass	Pass
116	XTX1N/P	116	Pass	Pass	Pass	117	XTX1N/P	117	Pass	Pass	Pass
118	XTX0N/P	118	+200mA	+200mA	+200mA	119	XTX0N/P	119	+200mA	+200mA	+200mA
120	XGPIO_D[4:5]	120	+150mA	+150mA	+150mA	121	XGPIO_D[4:5]	121	+150mA	+150mA	+150mA
122	XGPIO_D7	122	+150mA	+150mA	+150mA	125	XKOUT[0:3]	125	+150mA	+150mA	+150mA
126	XKOUT[0:3]	126	+150mA	+150mA	+150mA	127	XKOUT[0:3]	127	+150mA	+150mA	+150mA
128	XKOUT[0:3]	128	+150mA	+150mA	+150mA						

4. Raw Data - 2

Negative Current Trigger(Unit:mA)											
Test Pin Fail Current			#01	#02	#03	Test Pin Fail Current			#01	#02	#03
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
4	LDO_CAP12	4	Pass	Pass	Pass	6	XTEST[2:0]	6	Pass	Pass	Pass
7	XTEST[2:0]	7	Pass	Pass	Pass	8	XTEST[2:0]	8	Pass	Pass	Pass
9	XPS[2:0]	9	Pass	Pass	Pass	10	XPS[2:0]	10	Pass	Pass	Pass
11	XPS[2:0]	11	Pass	Pass	Pass	12	XnRST	12	Pass	Pass	Pass
13	XnCS	13	Pass	Pass	Pass	14	XnRD_EN	14	Pass	Pass	Pass
15	XnWR_RWN	15	Pass	Pass	Pass	16	XA0	16	Pass	Pass	Pass
17	XnWAIT	17	Pass	Pass	Pass	18	XDB[0:4]	18	Pass	Pass	Pass
19	XDB[0:4]	19	Pass	Pass	Pass	20	XDB[0:4]	20	Pass	Pass	Pass
21	XDB[0:4]	21	Pass	Pass	Pass	22	XDB[0:4]	22	Pass	Pass	Pass
25	XDB[5:15]	25	Pass	Pass	Pass	26	XDB[5:15]	26	Pass	Pass	Pass
27	XDB[5:15]	27	Pass	Pass	Pass	28	XDB[5:15]	28	Pass	Pass	Pass
29	XDB[5:15]	29	Pass	Pass	Pass	30	XDB[5:15]	30	Pass	Pass	Pass
31	XDB[5:15]	31	Pass	Pass	Pass	32	XDB[5:15]	32	Pass	Pass	Pass
33	XDB[5:15]	33	Pass	Pass	Pass	34	XDB[5:15]	34	Pass	Pass	Pass
35	XDB[5:15]	35	Pass	Pass	Pass	36	XnINTR	36	Pass	Pass	Pass
37	XnSFCS[0:1]	37	Pass	Pass	Pass	38	XnSFCS[0:1]	38	Pass	Pass	Pass
39	XSCK	39	Pass	Pass	Pass	40	XMOSI	40	Pass	Pass	Pass
41	XMISO	41	Pass	Pass	Pass	44	XMBA[1:0]	44	Pass	Pass	Pass
45	XMBA[1:0]	45	Pass	Pass	Pass	46	XMA[12:0]	46	Pass	Pass	Pass
47	XMA[12:0]	47	Pass	Pass	Pass	48	XMA[12:0]	48	Pass	Pass	Pass
49	XMA[12:0]	49	Pass	Pass	Pass	50	XMA[12:0]	50	Pass	Pass	Pass
51	XMA[12:0]	51	Pass	Pass	Pass	52	XMA[12:0]	52	Pass	Pass	Pass
53	XMA[12:0]	53	Pass	Pass	Pass	54	XMA[12:0]	54	Pass	Pass	Pass
55	XMA[12:0]	55	Pass	Pass	Pass	56	XMA[12:0]	56	Pass	Pass	Pass
57	XMA[12:0]	57	Pass	Pass	Pass	58	XMA[12:0]	58	Pass	Pass	Pass
59	XNMCS	59	Pass	Pass	Pass	60	XMCKE	60	Pass	Pass	Pass
61	XMCLK	61	Pass	Pass	Pass	63	LDO_CAP12	63	Pass	Pass	Pass
65	XnMCAS	65	Pass	Pass	Pass	66	XnMRAS	66	Pass	Pass	Pass
67	XnMWR	67	Pass	Pass	Pass	68	XMDQM0	68	Pass	Pass	Pass
69	XMD[0:5]	69	Pass	Pass	Pass	70	XMD[0:5]	70	Pass	Pass	Pass
71	XMD[0:5]	71	Pass	Pass	Pass	72	XMD[0:5]	72	Pass	Pass	Pass
73	XMD[0:5]	73	Pass	Pass	Pass	74	XMD[0:5]	74	Pass	Pass	Pass
77	XMD[6:7]	77	Pass	Pass	Pass	78	XMD[6:7]	78	Pass	Pass	Pass
79	XMDQM1	79	Pass	Pass	Pass	80	XMD[8:15]	80	Pass	Pass	Pass
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	Pass	Pass	Pass
83	XMD[8:15]	83	Pass	Pass	Pass	84	XMD[8:15]	84	Pass	Pass	Pass
85	XMD[8:15]	85	Pass	Pass	Pass	86	XMD[8:15]	86	Pass	Pass	Pass
87	XMD[8:15]	87	Pass	Pass	Pass	90	XPWM[0:1]	90	Pass	Pass	Pass
91	XPWM[0:1]	91	Pass	Pass	Pass	92	XKIN[0:4]	92	Pass	Pass	Pass
93	XKIN[0:4]	93	Pass	Pass	Pass	94	XKIN[0:4]	94	Pass	Pass	Pass
95	XKIN[0:4]	95	Pass	Pass	Pass	96	XKIN[0:4]	96	Pass	Pass	Pass
99	XGPIO_D[0:1]	99	Pass	Pass	Pass	100	XGPIO_D[0:1]	100	Pass	Pass	Pass
101	XGPIO_D6	101	Pass	Pass	Pass	102	XGPIO_D[2:3]	102	Pass	Pass	Pass
103	XGPIO_D[2:3]	103	Pass	Pass	Pass	106	LDO_CAP12	106	Pass	Pass	Pass

4. Raw Data - 2

Negative Current Trigger(Unit:mA)											
Test Pin Fail Current			#01	#02	#03	Test Pin Fail Current			#01	#02	#03
108	XTX3N/P	108	Pass	Pass	Pass	109	XTX3N/P	109	Pass	Pass	Pass
110	XTX2N/P	110	Pass	Pass	Pass	111	XTX2N/P	111	Pass	Pass	Pass
112	XCKN/P	112	Pass	Pass	Pass	113	XCKN/P	113	Pass	Pass	Pass
116	XTX1N/P	116	Pass	Pass	Pass	117	XTX1N/P	117	Pass	Pass	Pass
118	XTX0N/P	118	Pass	Pass	Pass	119	XTX0N/P	119	Pass	Pass	Pass
120	XGPIO_D[4:5]	120	Pass	Pass	Pass	121	XGPIO_D[4:5]	121	Pass	Pass	Pass
122	XGPIO_D7	122	Pass	Pass	Pass	125	XKOUT[0:3]	125	Pass	Pass	Pass
126	XKOUT[0:3]	126	Pass	Pass	Pass	127	XKOUT[0:3]	127	Pass	Pass	Pass
128	XKOUT[0:3]	128	Pass	Pass	Pass						

4. Raw Data - 2

V supply Over Voltage Test(Unit: V)											
Test Pin Fail Voltage			#01	#02	#03	Test Pin Fail Voltage			#01	#02	#03
3	VDD33	3	Pass	Pass	Pass	23	VDD33	23	Pass	Pass	Pass
42	VDD33	42	Pass	Pass	Pass	62	VDD33	62	Pass	Pass	Pass
75	VDD33	75	Pass	Pass	Pass	88	VDD33	88	Pass	Pass	Pass
97	VDD33	97	Pass	Pass	Pass	104	VDD33	104	Pass	Pass	Pass
114	AVDD33	114	Pass	Pass	Pass	123	VDD33	123	Pass	Pass	Pass

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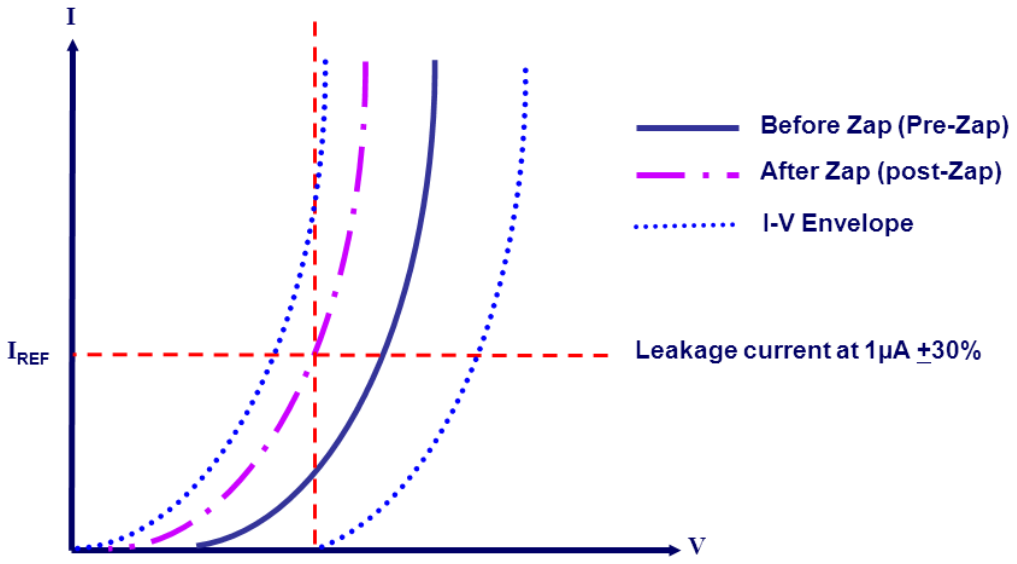
Positive Current Trigger(Unit: +125mA)											
Test Pin Fail Current			#01	#02	#03	Test Pin Fail Current			#01	#02	#03
1	XI	1	Pass	Pass	Pass	2	XO	2	Pass	Pass	Pass
4	LDO_CAP12	4	Pass	Pass	Pass	6	XTEST[2:0]	6	Pass	Pass	Pass
7	XTEST[2:0]	7	Pass	Pass	Pass	8	XTEST[2:0]	8	Pass	Pass	Pass
9	XPS[2:0]	9	Pass	Pass	Pass	10	XPS[2:0]	10	Pass	Pass	Pass
11	XPS[2:0]	11	Pass	Pass	Pass	12	XnRST	12	Pass	Pass	Pass
13	XnCS	13	Pass	Pass	Pass	14	XnRD_EN	14	Pass	Pass	Pass
15	XnWR_RWN	15	Pass	Pass	Pass	16	XA0	16	Pass	Pass	Pass
17	XnWAIT	17	Pass	Pass	Pass	18	XDB[0:4]	18	Pass	Pass	Pass
19	XDB[0:4]	19	Pass	Pass	Pass	20	XDB[0:4]	20	Pass	Pass	Pass
21	XDB[0:4]	21	Pass	Pass	Pass	22	XDB[0:4]	22	Pass	Pass	Pass
25	XDB[5:15]	25	Pass	Pass	Pass	26	XDB[5:15]	26	Pass	Pass	Pass
27	XDB[5:15]	27	Pass	Pass	Pass	28	XDB[5:15]	28	Pass	Pass	Pass
29	XDB[5:15]	29	Pass	Pass	Pass	30	XDB[5:15]	30	Pass	Pass	Pass
31	XDB[5:15]	31	Pass	Pass	Pass	32	XDB[5:15]	32	Pass	Pass	Pass
33	XDB[5:15]	33	Pass	Pass	Pass	34	XDB[5:15]	34	Pass	Pass	Pass
35	XDB[5:15]	35	Pass	Pass	Pass	36	XnINTR	36	Pass	Pass	Pass
37	XnSFCS[0:1]	37	Pass	Pass	Pass	38	XnSFCS[0:1]	38	Pass	Pass	Pass
39	XSCK	39	Pass	Pass	Pass	40	XMOSI	40	Pass	Pass	Pass
41	XMISO	41	Pass	Pass	Pass	44	XMBA[1:0]	44	Pass	Pass	Pass
45	XMBA[1:0]	45	Pass	Pass	Pass	46	XMA[12:0]	46	Pass	Pass	Pass
47	XMA[12:0]	47	Pass	Pass	Pass	48	XMA[12:0]	48	Pass	Pass	Pass
49	XMA[12:0]	49	Pass	Pass	Pass	50	XMA[12:0]	50	Pass	Pass	Pass
51	XMA[12:0]	51	Pass	Pass	Pass	52	XMA[12:0]	52	Pass	Pass	Pass
53	XMA[12:0]	53	Pass	Pass	Pass	54	XMA[12:0]	54	Pass	Pass	Pass
55	XMA[12:0]	55	Pass	Pass	Pass	56	XMA[12:0]	56	Pass	Pass	Pass
57	XMA[12:0]	57	Pass	Pass	Pass	58	XMA[12:0]	58	Pass	Pass	Pass
59	XNMCS	59	Pass	Pass	Pass	60	XMCKE	60	Pass	Pass	Pass
61	XMCLK	61	Pass	Pass	Pass	63	LDO_CAP12	63	Pass	Pass	Pass
65	XnMCAS	65	Pass	Pass	Pass	66	XnMRAS	66	Pass	Pass	Pass
67	XnMWR	67	Pass	Pass	Pass	68	XMDQM0	68	Pass	Pass	Pass
69	XMD[0:5]	69	Pass	Pass	Pass	70	XMD[0:5]	70	Pass	Pass	Pass
71	XMD[0:5]	71	Pass	Pass	Pass	72	XMD[0:5]	72	Pass	Pass	Pass
73	XMD[0:5]	73	Pass	Pass	Pass	74	XMD[0:5]	74	Pass	Pass	Pass
77	XMD[6:7]	77	Pass	Pass	Pass	78	XMD[6:7]	78	Pass	Pass	Pass
79	XMDQM1	79	Pass	Pass	Pass	80	XMD[8:15]	80	Pass	Pass	Pass
81	XMD[8:15]	81	Pass	Pass	Pass	82	XMD[8:15]	82	Pass	Pass	Pass
83	XMD[8:15]	83	Pass	Pass	Pass	84	XMD[8:15]	84	Pass	Pass	Pass
85	XMD[8:15]	85	Pass	Pass	Pass	86	XMD[8:15]	86	Pass	Pass	Pass
87	XMD[8:15]	87	Pass	Pass	Pass	90	XPWM[0:1]	90	Pass	Pass	Pass
91	XPWM[0:1]	91	Pass	Pass	Pass	92	XKIN[0:4]	92	Pass	Pass	Pass
93	XKIN[0:4]	93	Pass	Pass	Pass	94	XKIN[0:4]	94	Pass	Pass	Pass
95	XKIN[0:4]	95	Pass	Pass	Pass	96	XKIN[0:4]	96	Pass	Pass	Pass
99	XGPIO_D[0:1]	99	Pass	Pass	Pass	100	XGPIO_D[0:1]	100	Pass	Pass	Pass
101	XGPIO_D6	101	Pass	Pass	Pass	102	XGPIO_D[2:3]	102	Pass	Pass	Pass
103	XGPIO_D[2:3]	103	Pass	Pass	Pass	106	LDO_CAP12	106	Pass	Pass	Pass

4. Raw Data - 2

Positive Current Trigger(Unit: +125mA)											
Test Pin Fail Current			#01	#02	#03	Test Pin Fail Current			#01	#02	#03
108	XTX3N/P	108	Pass	Pass	Pass	109	XTX3N/P	109	Pass	Pass	Pass
110	XTX2N/P	110	Pass	Pass	Pass	111	XTX2N/P	111	Pass	Pass	Pass
112	XCKN/P	112	Pass	Pass	Pass	113	XCKN/P	113	Pass	Pass	Pass
116	XTX1N/P	116	Pass	Pass	Pass	117	XTX1N/P	117	Pass	Pass	Pass
118	XTX0N/P	118	Pass	Pass	Pass	119	XTX0N/P	119	Pass	Pass	Pass
120	XGPIO_D[4:5]	120	Pass	Pass	Pass	121	XGPIO_D[4:5]	121	Pass	Pass	Pass
122	XGPIO_D7	122	Pass	Pass	Pass	125	XKOUT[0:3]	125	Pass	Pass	Pass
126	XKOUT[0:3]	126	Pass	Pass	Pass	127	XKOUT[0:3]	127	Pass	Pass	Pass
128	XKOUT[0:3]	128	Pass	Pass	Pass						

5. APPENDIX-1 (PASS/FAIL CRITERIA)

FAILURE CRITERIA	**Device no longer meets the parts drawing requirements using parametric (1.4X INOM or INOM +10mA whichever is greater), functional or IV requirements.**
Note	**For custom designed ESD testing customers may select variation in Idd, and leakage current as criteria to determine pass/fail results of ESD testing.**



Pass/Fail Criteria:
Variation of Leakage Current and I-V Shift in Pre-Zap and Post-Zap curves

6. APPENDIX-2 (ESD INSTRUMENTATION AT MA-TEK)

No.	Test Tools	Vendors	System Specification
1	Zapmaster	Thermo Keytek	256 Pin Count, ESD Pulse 50 V to 8 KV
2	MK2	Thermo Keytek	768 Pin Count, ESD Pulse 10 V to 8 KV
3	MK1	Thermo Scientific	256 Pin Count, ESD Pulse 10 V to 8 KV
4	CDM Tester	Oryx Orion	100 V to 2 KV
5	ESD Gun	Noiseken	Voltage = 1 V to 1 KV, Current = 10 nA to 20 A
6	High Temp. Test Module	Thermonics	Maximum temperature = 150°C.
7	TLP Tester	Thermo Scientific	Voltage = 1 V to 1 KV, Current = 10 nA to 20 A

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